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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/506,888	09/07/2004	Zhenyu Tang	9896-050/NP	6751

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EXAMINER	
PHAN, HANH	
ART UNIT	**PAPER NUMBER**
2613	
MAIL DATE	**DELIVERY MODE**
05/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/506,888	TANG, ZHENYU	
	Examiner	Art Unit	
	Hanh Phan	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Stewart et al (US Patent No. 7,155,133).

Regarding claims 1 and 4, referring to Figures 4-10, Stewart et al teaches an optical receiver (i.e., an optical receiver, Fig. 4) module with digital adjustment includes an optical-electrical converter circuit (i.e., avalanche photodiode 206, Fig. 4), a voltage output circuit of optical power detection (i.e., current mirror monitor 204, Fig. 4), and a bias voltage adjusting circuit (i.e., APD voltage supply 202, Fig. 4) that comprises a DC/DC voltage boost circuit (i.e., col. 6, lines 41-67, col. 7, lines 1-67, col. 8, lines 1-67, col. 9, lines 1-32 and col. 10, lines 1-32 and see abstract section); it is further included that,

a digital adjusting unit (i.e., controller IC 110, Fig. 4) digitally adjusting the DC/DC voltage boost circuit to output different voltage (i.e., col. 6, lines 41-67, col. 7, lines 1-67, col. 8, lines 1-67, col. 9, lines 1-32 and col. 10, lines 1-32 and see abstract section);

an A/D converter (i.e., A-D input and D-A output, Fig. 4) converting both an analog voltage of a measured working temperature of an optical detector into a digital data and an analog voltage of a measured optical power into a digital data, which are used for controlling the digital adjustment circuit, monitoring a bias voltage of the optical detector, making temperature compensation and dark current compensation at different temperature (i.e., Figs. 4-10, col. 6, lines 41-67, col. 7, lines 1-67, col. 8, lines 1-67, col. 9, lines 1-32 and col. 10, lines 1-32 and see abstract section);

a memory (i.e., the controller 110 includes a memory, Fig. 4, and see abstract section) storing parameters of the optical receiver module as a basis for adjustment (i.e., Figs. 4-10, col. 6, lines 41-67, col. 7, lines 1-67, col. 8, lines 1-67, col. 9, lines 1-32 and col. 10, lines 1-32 and see abstract section).

Regarding claims 2, 3, Stewart et al further teaches the digital adjusting unit (i.e., controller 110, Fig. 4) is a D/A converter or a digital potentiometer (i.e., Figs. 4-10, col. 6, lines 41-67, col. 7, lines 1-67, col. 8, lines 1-67, col. 9, lines 1-32 and col. 10, lines 1-32 and see abstract section).

Regarding claim 5, Stewart et al further teaches storing DA values during dark current zero-adjustment comprises: setting a DA value; converting an analog output Optical Power Measurement (OPM) of an operation amplifier for optical power detection into a digital data by the A/D converter, and then sending to the CPU; the CPU detecting whether the digital data satisfies dark current zero-adjustment requirement; if it is, storing the set DA value in the memory, otherwise returning to step A1 (i.e., Figs. 4-10, col. 6, lines 41-67, col. 7, lines 1-67, col. 8, lines 1-67, col. 9, lines 1-32 and col. 10, lines 1-32 and see abstract section).

Regarding claim 6, Stewart et al further teaches storing DA values during optical detector bias voltage adjustment comprises: setting a DA value; converting an optical detector bias voltage by the A/D converter into a digital data, and then sending to the CPU; the CPU detecting whether the digital data satisfies the optical detector bias voltage requirement; if it is, storing the set DA value in the memory, otherwise, returning

then real-timely displaying (i.e., Figs. 4-10, col. 6, lines 41-67, col. 7, lines 1-67, col. 8, lines 1-67, col. 9, lines 1-32 and col. 10, lines 1-32 and see abstract section).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

sakamoto et al (US Patent No. 6,643,472) discloses APD bias circuit.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hanh Phan whose telephone number is (571)272-3035.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan, can be reached on (571)272-3022. The fax phone number for the organization where this application or proceeding is assigned is (571)273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-4700.

HANH PHAN
PRIMARY EXAMINER

to step A4 (i.e., Figs. 4-10, col. 6, lines 41-67, col. 7, lines 1-67, col. 8, lines 1-67, col. 9, lines 1-32 and col. 10, lines 1-32 and see abstract section).

Regarding claim 7, Stewart et al further teaches storing AD values during standardizing optical power detection comprises: inputting a standard light source; determining a corresponding AD values with 0.5 dBm optical power space within optical power detection scope, and storing the determined AD values in the memory (i.e., Figs. 4-10, col. 6, lines 41-67, col. 7, lines 1-67, col. 8, lines 1-67, col. 9, lines 1-32 and col. 10, lines 1-32 and see abstract section).

Regarding claim 8, Stewart et al further teaches storing AD values during standardizing temperature measurement comprises: calculating corresponding relationship between a temperature and the AD value; determining a corresponding AD values with 5°C space within a certain temperature scope, storing the determined AD values in the memory (i.e., Figs. 4-10, col. 6, lines 41-67, col. 7, lines 1-67, col. 8, lines 1-67, col. 9, lines 1-32 and col. 10, lines 1-32 and see abstract section).

Regarding claim 9, Stewart et al further teaches in the memory storing parameters of the optical receiver module including type of the optical receiver module, production date, receiving sensitivity, overload point and maximum bias voltage of the optical detector during test (i.e., Figs. 4-10, col. 6, lines 41-67, col. 7, lines 1-67, col. 8, lines 1-67, col. 9, lines 1-32 and col. 10, lines 1-32 and see abstract section).

Regarding claim 10, Stewart et al further teaches reading out a digital data of bias voltage of the optical detector converted by an A/D converter through the CPU, and